Amendments to the Claims

Please amend Claims 1, 4. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (Currently Amended) A method for storing a non-binary width data structure per logical row in a memory comprising the steps of:

segmenting the non-binary width data structure into plural segments and physically mapping the segments into a memory structure smaller than would be required for the non-binary width data structure without segmenting; and

mapping a logical address into the physically arranged plural segments, the logical address identifying a single logical row in the memory for storing one non-binary width data structure.

2. (Original) The method as claimed in Claim 1 wherein the segments are the same size.

3. (Original) The method as claimed in Claim 2 wherein the width of the segment is 21-bits, and the non-binary width data structure has 16 segments.

4. (Currently Amended) An apparatus for storing a non-binary width data structure, the ~~memory~~ apparatus comprising:

memory, and

mapper logic ~~plural segments~~ which ~~segment~~ segments the non-binary width data structure into plural segments, ~~and~~ physically ~~map~~ maps the non-binary width data structure into ~~a~~ the memory ~~structure~~, the memory smaller than would be required for the non-binary width.data structure without segmenting~~;~~ and

~~mapper logic which~~ maps a logical address into the physically arranged plural segments, the logical address identifying a single logical row in the memory for storing one non-binary width data structure.

5. (Original) The apparatus as claimed in Claim 4 wherein the segments are the same size.

6. (Original) The apparatus as claimed in Claim 5 wherein the width of the segment is 21-bits, and the non-binary width data structure has 16 segments.

7. (Original) An apparatus for storing a non-binary width data structure per logical row, the non-binary width data structure including a plurality of entries, the memory comprising:

a first binary memory block having 2^n logical rows, each first binary memory block logical row storing a portion of the non-binary width data structure;

a second binary memory block having 2^{n-1} logical rows, each second binary memory block logical row storing a first other portion of the non-binary width data structure for the first 2^{n-1} logical rows of the first binary memory block and a second other portion of the non-binary width data structure for the second 2^{n-1} logical rows of the first binary memory block; and

mapper logic which maps a logical address identifying a logical row and an entry in the logical row to a physical address for the entry in the first binary memory block or the second binary memory block.

8. (Original) The apparatus as claimed in Claim 7 wherein the portion of the non-binary width data structure stores twelve entries, the first other portion stores four entries and the second other portion stores four entries.

9. (Original) The apparatus as claimed in Claim 8 wherein the width of the entry is 21-bits, the non-binary width data structure stores 16 entries and n is 15.

10. (Original) The apparatus as claimed in Claim 7 wherein the first binary memory block and the second binary memory block are binary macro cells.

11. (Original) The apparatus as claimed in Claim 7 wherein the first binary memory block and the second binary memory block are portions of a memory macro cell.

12. (Original) The apparatus as claimed in Claim 7 comprising:

a multiplexor which selects the entry in the logical row.

13. (Original) A method for storing a non-binary width data structure per logical row in a memory, the non-binary width data structure including a plurality of entries, the method comprising the steps of:

providing a first binary memory block, the first binary memory block including 2^n logical rows;

providing a second binary memory block, the second binary memory block including 2^{n-1} logical rows;

mapping a logical address identifying a logical row and an entry in the logical row to a physical address for the entry stored in a single location in the first binary memory block or the second binary memory block;

storing a portion of the non-binary width data structure in a first binary memory block logical row; and

storing a first other portion of the non-binary width data structure for the first 2^{n-1} logical rows of the first binary memory block and a second other portion of the non-binary width data structure for the second 2^{n-1} logical rows of the first binary memory block in a second binary memory block logical row.

14. (Original) The method as claimed in Claim 13 wherein the portion of the non-binary width data structure stores twelve entries, the first other portion stores four entries and the second other portion stores four entries.

15. (Original) The method as claimed in Claim 14 wherein the width of the entry is 21-bits, the non-binary data structure stores 16 entries and n is 15.

16. (Original) The method as claimed in Claim 13 wherein the first binary memory block and

the second binary memory block are binary macro cells.

17. (Original) The apparatus as claimed in Claim 13 wherein the first binary memory block and the second binary memory block are portions of a memory macro cell.

18. (Original) An apparatus for storing a non-binary width data structure per logical row, the non-binary width data structure including a plurality of entries, the apparatus comprising:

a first binary memory block having 2^n logical rows, each first binary memory block logical row storing a portion of the non-binary width data structure;

a second binary memory block having 2^{n-1} logical rows, each second binary memory block logical row storing a first other portion of the non-binary width data structure for the first 2^{n-1} logical rows of the first binary memory block and a second other portion of the non-binary width data structure for the second 2^{n-1} logical rows of the first binary memory block; and

means for mapping a logical address identifying a logical row and an entry in the logical row to a physical address for the entry in the first binary memory block or the second binary memory block.

19. (Original) The apparatus as claimed in Claim 18 wherein the portion of the non-binary width data structure stores twelve entries, the first other portion stores four entries and the second other portion stores four entries.

20. (Original) The apparatus as claimed in Claim 19 wherein the width of the entry is 21-bits, the non-binary width data structure stores 16 entries and n is 15.

21. (Original) The apparatus as claimed in Claim 18 wherein the first binary memory block and the second binary memory block are binary memory macro cells.

22. (Original) The apparatus as claimed in Claim 18 further comprising:

means for selecting the entry in the logical row.

23. (Original) The apparatus as claimed in Claim 18 wherein the first binary memory block and the second binary memory block are portions of a memory macro cell.